Programmable On-Chip Photonic Signal Processor Based on a Microdisk Resonator Array

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Abstract—A programmable on-chip photonic signal processor based on a silicon photonic microdisk resonator array is proposed and experimentally demonstrated. The processor has a two-dimensional mesh network structure with multiple input and multiple output ports. In each mesh cell, two identical thermally-tunable high-Q microdisk resonators (MDRs) are used for routing and processing the optical signal, and a low-loss waveguide crossing is employed at the waveguide intersection to enable low-crosstalk optical transmission. By programming the DC voltages applied to the MDRs, the processor can be reconfigured with diverse circuit topologies to perform multiple array signal processing functions. An 8 × 8 programmable signal processor is designed, fabricated and characterized. By controlling the DC voltages, an on-chip tunable optical delay line based on 8 MDRs cascaded in an all-pass filter configuration is experimentally demonstrated. Thanks to scalable mesh structure of the proposed processor, the entire device holds a promising potential for strong reconfigurability and parallel computing with low power consumption.

Keywords—silicon photonics, photonic processing of microwave signals, optical delay line.

I. Introduction

Microwave photonics (MWP) has been envisioned as a disruptive technology for the generation, transmission, processing and control of high-frequency and broadband microwave signals for applications such as next-generation wireless telecommunications (5G), agile radar and new-generation electronic warfare [1, 2]. As a topic of interest, photonic microwave signal processing has been extensively studied in the last 20 years and considerable progress has been made in the implementation of various signal processing functions [3, 4]. These signal processing functions include spectral filtering, phase shifting, temporal integration, temporal differentiation, Hilbert transformation, pulse shaping, frequency discrimination, tunable true time delay, and phased array beamforming.

With the rapid development of photonic integrated circuits (PICs), it is highly desirable to realize microwave signal processing systems integrated on a chip with the use of the PICs to overcome the limitations existing in discrete microwave photonic signal processing systems. Recently, numerous integrated solutions to implement microwave signal processing have been demonstrated based on different PIC platforms [5, 6]. However, most of the demonstrations were implemented based on task-oriented designs. For large-scale practical applications, it is highly desired that a universal signal processor whose functionality could be electronically reconfigured, similar to a field-programmable gate array (FPGA) signal processor, could be achieved. To meet this challenge, extensive effort has been directed to the study and implementation of programmable signal processors. Zhuang et al. firstly proposed an on-chip programmable signal processor that consists of a grid of tunable Mach–Zehnder couplers interconnected in a two-dimensional mesh network [7]. Such a device is able to be programmed into many different circuit topologies and thereby provides a diversity of functions. Inspired by this approach, other mesh topologies were proposed including hexagonal and triangular-shaped meshes [8]. However, the key problem associated with the Mach–Zehnder coupler-based approach is the large optical loss and large chip size. Compared to a Mach-Zehnder coupler, on-chip optical cavity has the key advantages including low loss, small footprint, and strong wavelength selectivity.

In this paper, we propose a programmable microdisk resonator array photonic signal processor on a silicon photonic chip for microwave signal processing. The programmable processor has a two-dimensional mesh network structure with multiple input and multiple output ports. In each mesh cell two identical thermally-tunable high-Q microdisk resonators (MDRs) are used for routing and processing the optical signal, and a low-loss waveguide crossing is employed at the waveguide intersection to enable low-crosstalk optical transmission. By programming the DC voltages applied to the MDRs, the processor could be reconfigured to have diverse circuit topologies to perform multiple array signal processing functions. An 8 × 8 programmable signal processor is designed, fabricated, and characterized. By controlling the DC voltages, an on-chip tunable optical delay line based on 8 MDRs cascaded in all-pass filter configuration is experimentally demonstrated.

II. Microdisk Resonator Array Signal Processor

Fig. 1(a) shows our proposed programmable array photonic signal processor on a silicon photonic chip for microwave signal processing. The programmable processor has a two-dimensional mesh network structure with multiple input and multiple output ports. In each mesh cell two identical thermally-tunable high-Q MDRs are used for routing and
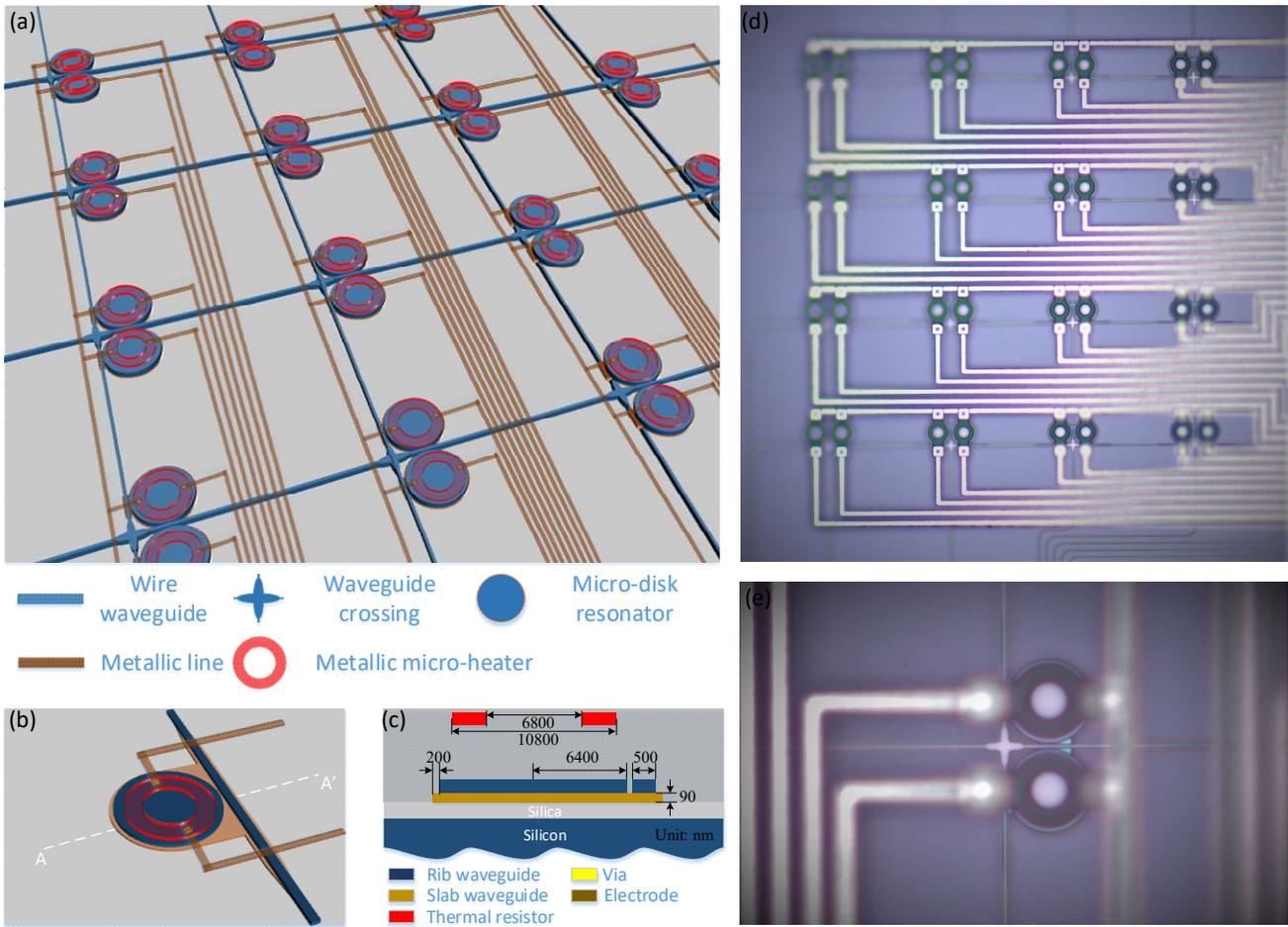
Fig. 1. (a) Schematic layout of the proposed programmable MDR array photonic signal processor; (b) perspective view of the thermally-tunable MDR; (c) cross-sectional view of the MDR; (d) chip prototype of an 8 × 8 MDR array photonic signal processor; and (e) zoom-in view of the mesh cell of the fabricated processor.

processing the optical signal, and a low-loss waveguide crossing is employed to enable low-crosstalk optical transmission at the waveguide intersection. Fig. 1(b) shows an MDR, which incorporates an additional slab waveguide to wrap the disk and bus waveguide, with an aim to reduce the sidewall roughness, to increase the light confinement capacity and optical coupling. For thermal tuning, a metallic micro-heater is placed on top of the disk. Fig. 1(c) shows a cross-sectional view of the MDR along the white dashed line AA' in Fig. 1(b). A high-resistivity metallic micro-heater is placed on top of the disk. Fig. 1(d) is the image of the fabricated 8 × 8 photonic signal processor. Fig. 1(e) gives the zoom-in view of the mesh cell, in which a low-loss and low-crosstalk waveguide crossing with a 1 × 1 multimode-interference (MMI) configuration is used for guiding the optical signal at the intersection [9]. By programming the DC voltages applied to the MDRs, the processor could be reconfigured to have diverse circuit topologies to perform multiple array signal processing functions.

Fig. 2(a) shows schematic of a mesh cell. When an incident lightwave signal is launched from port 1, thanks to the wavelength selectivity of the MDR, by independently controlling the DC voltages applied to the micro-heaters of the MDRs, the input lightwave signal would be routed to any desired port or split into three ports at arbitrary splitting ratios.

Fig. 2(b) shows the image of a chip consisting of a single mesh cell. Four grating couplers with a center-to-center spacing of 127 μm are used. Fig. 2(c) shows the zoom-in view of the waveguide intersection. The optical performance of the single mesh cell is evaluated, which is done by using an optical vector analyzer (LUNA OVA CTe) to measure the transmission spectrum. Fig. 2(d), (e) and (f) shows the measured transmission spectral responses of the channel from Port 1 to Port 2, Port 1 to Port 3, and Port 1 to Port 4, respectively. Thanks to wavelength selectivity of the MDRs, the channel from Port 1 to Port 3 has a transmission notch, while the other two channels have a transmission peak. As can be seen, first-order and second-order whispering-gallery-modes (WGMs) are effectively excited in the disk. Then, the tunability of the single cell is evaluated, which is done by applying DC voltages to the micro-heaters on top of the MDRs. Firstly, the DC voltage is applied to Disk 1 and is increased. Fig. 2 (g), (h) and (i) shows the measured transmission spectral shift of the channel from Port 1 to Port 2, Port 1 to Port 3, and Port 1 to Port 4, respectively. To clearly shows the wavelength shift, the three figures shows zoom-in view of the $WGM_{+1,63}$ resonance. Since the voltage is applied to MDR 1, the resonance wavelength of MDR 1 is thermally tuned. In addition, since the two MDRs are close to each other, during the tuning of MDR 1, MDR 2 also
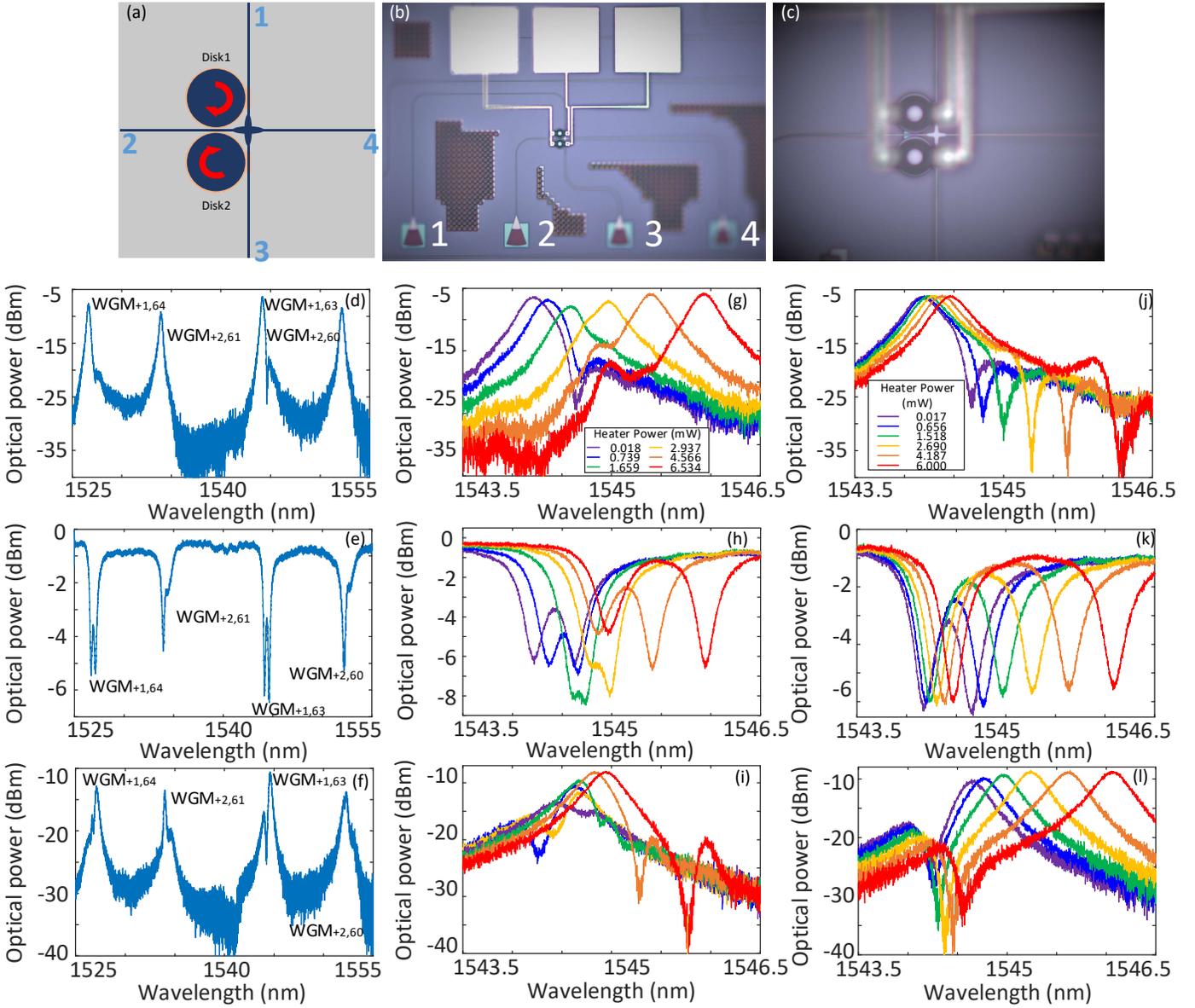
Fig. 2. (a) Schematic of the mesh unit; (b) chip prototype of the single mesh unit; (c) zoom-in view of the thermally-tunable MDRs; (d) measured transmission spectrum of the channel from Port 1 to Port 2; (e) measured transmission spectrum of the channel from Port 1 to Port 3; (f) measured transmission spectrum of the channel from Port 1 to Port 4; (g), (h) and (i) is the transmission spectrum shift when a DC voltage is applied to Disk 1; and, (j), (k) and (l) is the transmission spectrum shift when a DC voltage is applied to Disk 2.

has a small wavelength shift, which could be alleviated by increasing the spacing between the two MDRs. Then, the DC voltage is applied to Disk 2 and is increased. Fig. 2 (j), (k) and (l) shows the measured transmission spectral shift of the channel from Port 1 to Port 2, Port 1 to Port 3, and Port 1 to Port 4, respectively. Again, since the voltage is applied to MDR 2, the resonance wavelength of MDR 2 is thermally tuned. By independently controlling the DC voltages applied to the MDRs, two MDRs could tuned independently, which can be used to route the different wavelength lightwave signal. In addition, thanks to the wavelength selectivity and optical-confining capacity, the MDR could act as a basic functional element.

Then, the optical performance of an 8 × 8 array signal processor is evaluated. Fig. 3(a)-(d) shows the measured

transmission spectrum of the transmission channels from Port 4 to Port 9, Port 3 to Port 10, Port 7 to Port 14, Port 8 to Port 13, respectively. As can be seen, the four transmission channels have similar spectral responses, which confirms the channel uniformity of the processor. Slight spectrum difference between the channels is observed, which is caused due to fabrication imperfections. Fig. 3(e)-(h) shows the measured spectral response of the drop channel from Port 4 to Port 5, Port 4 to Port 6, Port 4 to Port 7, Port 4 to Port 8, respectively. As can be seen, the four drop channels have multiple peaks. By controlling the DC voltages applied to the MDRs, the peak locations could be shifted, which could be used for optical routing.
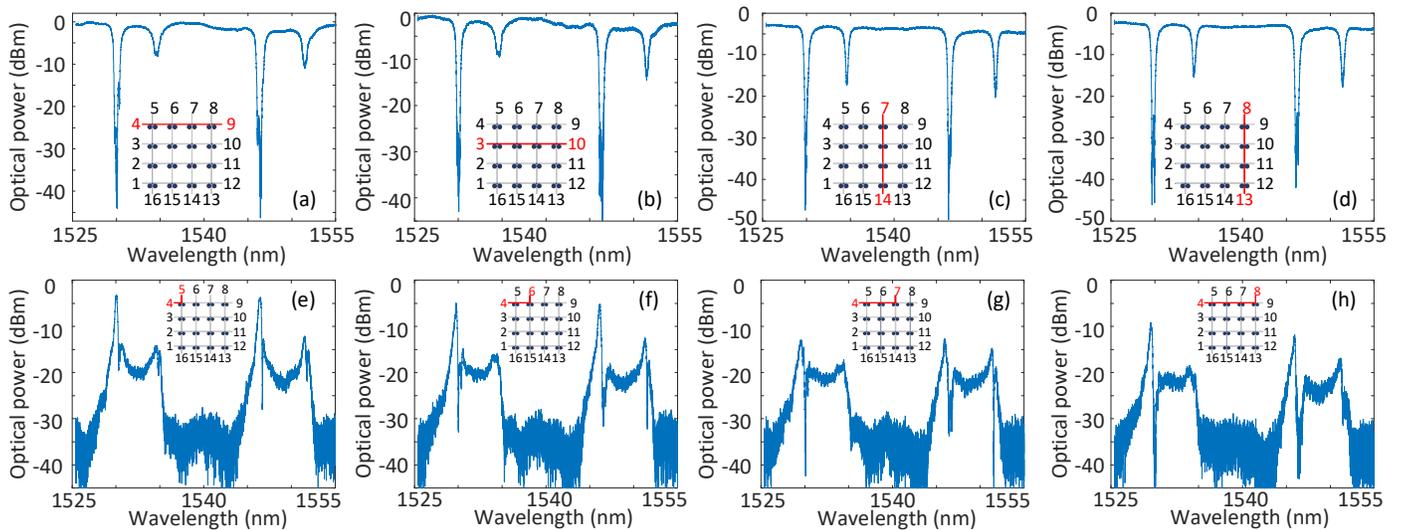
Fig. 3. Measured transmission spectrums of the different channels of the fabricated 8 × 8 array signal processor. (a) Port 4 to Port 9; (b) Port 3 to Port 10; (c) Port 7 to Port 14; (d) Port 8 to Port 13; (e) Port 4 to Port 5; (f) Port 4 to Port 6; (g) Port 4 to Port 7; and (10) Port 4 to Port 8.

III. TUNABLE OPTICAL DELAY LINE

Due to a strong light-confinement capacity of the optical cavity, the MDR has a strong dispersion near the center of the notch and thus a large group delay, which could be used as an optical delay line. By controlling the DC voltages, an on-chip tunable optical delay line based on 8 MDRs cascaded in all-pass filter configuration in the channel from Port 4 to Port 9 is experimentally demonstrated. By tuning the bias voltages, a tunable optical delay line is generated. Fig. 4(a) shows the measured transmission spectrum shifting of the delay line and Fig. 4(b) shows the group delay tuning by controlling the DC voltages. As can be seen, the tunable delay line has a bandwidth of 1.3 nm and a time delay up to 2500 ps.
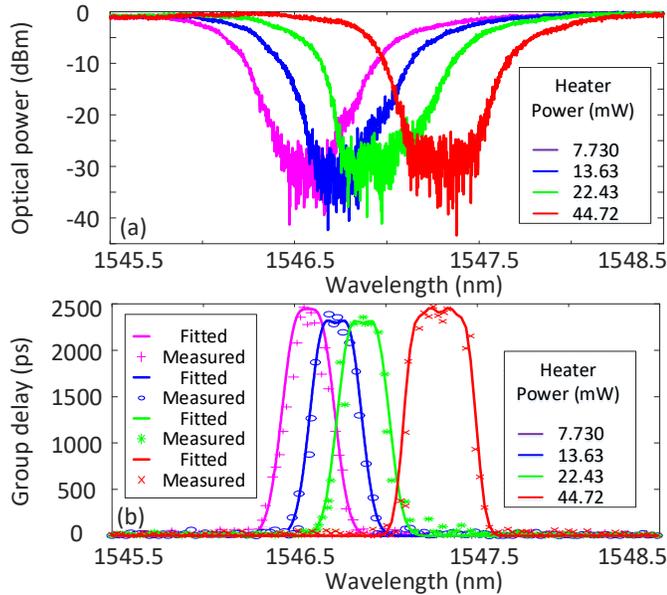

Fig. 4. (a) Delay line tunability when the channel from Port 4 to Port 9 is used; and (b) thermal tunabilty of the group delay.

IV. CONCLUSION

A programmable array photonic signal processor based on a silicon photonic MDR array was proposed. The programmable processor had a two-dimensional mesh network structure with multiple input and multiple output ports. By programming the DC voltages applied to the MDRs, the processor could be reconfigured to have diverse circuit topologies to perform multiple array signal processing functions. An 8 × 8 programmable signal processor was designed, fabricated and characterized. By controlling the DC voltages, an on-chip tunable optical delay line based on 8 cascaded MDRs in all-pass filter configuration was experimentally demonstrated.

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